We claim:

1. An electrically programmable, single-cell memory element, comprising:

a volume of phase-change memory material; and

a first and a second contact for supplying an electrical signal to said memory material, said first contact comprising a conductive sidewall spacer.

2. The memory element of claim 1, wherein said conductive sidewall spacer is adjacent to said memory material.

3. The memory element of claim 1, wherein said conductive sidewall spacer has an edge adjacent to said memory material.

4. The memory element of claim 1, wherein the top of said conductive sidewall spacer is adjacent to said memory material.

5. The memory element of claim 4, wherein said memory material is a substantially horizontally disposed memory layer formed above said conductive sidewall spacer.

6. The memory element of claim 1, wherein said conductive sidewall spacer is formed on a sidewall surface.

7. The memory element of claim 6, wherein said sidewall surface is selected from the group consisting of trench sidewall surface, via sidewall surface, and pillar sidewall surface.

8. The memory element of claim 6, wherein said conductive sidewall spacer is formed by depositing at least one contact layer onto a sidewall surface, and etching said at least one contact layer.

9. The memory element of claim 8, wherein said at least one contact layer is a first contact layer and a second contact layer, wherein said first contact layer is deposited onto said sidewall surface and said second contact layer is deposited onto said first contact layer.

10. The memory element of claim 8, wherein said depositing is conformal depositing.

11. The memory element of claim 8, wherein said etching is anisotropic etching.

12. The memory element of claim 8, wherein the resistivity of said first contact layer is less than the resistivity of said second contact layer.

13. The memory element of claim 1, wherein said conductive sidewall spacer comprises a first sidewall layer, and a second sidewall layer formed on said first sidewall layer.

14. The memory element of claim 13, wherein the resistivity of said first sidewall layer is less than the resistivity of said first sidewall layer.

15. The memory element of claim 13, wherein said first sidewall layer is adjacent to said memory material.

16. The memory element of claim 15, wherein said second sidewall layer is remote to said memory material.

17. The memory element of claim 4, wherein the top of said second sidewall layer is adjacent to said memory material.

18. The memory element of claim 11, wherein the top of said first sidewall layer is remote to said memory material.

19. The memory element of claim 1, wherein said conductive sidewall spacer has a narrowed width adjacent said memory material.

20. The memory element of claim 1, wherein said volume of memory material includes at least one chalcogen.

21. The memory element of claim 20, wherein said at least one chalcogen is selected from the group consisting of Te, and Se.

22. The memory element of claim 20, wherein said memory material further includes at least one element selected from the group consisting of Ge, Sb, Bi, Pb, Sn, As, S, Si, P, O, and mixtures or alloys thereof.

23. The memory element of claim 20, wherein said memory material further includes at least one transition metal element.

24. An electrically operated memory element, comprising:

a volume of phase-change memory material; and

a first and a second contact for supplying an electrical signal to said memory material, said first contact comprising a contact layer having an edge adjacent to said volume of memory material.

25. The memory element of claim 24, wherein said contact layer is a thin-film layer.

26. The memory element of claim 24, wherein said contact layer is substantially vertically disposed.

27. The memory element of claim 24, wherein said contact layer is planar.

28. The memory element of claim 27, wherein said contact layer is substantially horizontally disposed.

29. The memory element of claim 24, wherein said contact layer is formed on a sidewall surface.

30. The memory element of claim 29, wherein said sidewall surface is chosen from the group consisting of trench sidewall surface, via sidewall surface, and pillar sidewall surface.

31. The memory element of claim 24, wherein said first contact is a conductive sidewall spacer.

32. The memory element of claim 24, wherein said contact layer is is cup-like surface having a open end adjacent said memory material.

33. The memory element of claim 24, wherein the area of contact between said contact layer and said memory material is annular.

34. The memory element of claim 24, wherein said edge encircles a cross-sectional slice of said memory material.

35. The memory element of claim 24, wherein said volume of memory material includes at least one chalcogen.

36. The memory element of claim 35, wherein said at least one chalcogen is selected from the group consisting of Te, and Se.

37. The memory element of claim 35, wherein said memory material further includes at least one element selected from the group consisting of Ge, Sb, Bi, Pb, Sn, As, S, Si, P, O, and mixtures or alloys thereof.

38. The memory element of claim 35, wherein said memory material further includes at least one transition metal element.

39. An electrically programmable, single-cell memory element, comprising:

a volume of phase-change memory material; and

a first and a second contact for supplying an electrical signal to said memory material, at least one of said contacts adapted to maximize the current density adjacent said memory material, and to minimize the thermal energy flowing from said memory material to said at least one contact.

40. A method of fabricating an electrically operated memory array having a cell area less than $8F^2$, the method comprising three or less masking steps in addition to the number of masking steps used for a CMOS process flow.

41. A method of fabricating an electrically operated memory array having a cell area less than $6F^2$, the method comprising three or less masking steps in addition to the number of masking steps used for a CMOS process flow.

42. A method of fabricating a non-charge-measurement, electrically operated memory array, comprising three or less masking steps in addition to the number of masking steps used for a CMOS process flow.

43. A method of fabricating a non-charge-storage, electrically operated memory array, comprising three or less masking steps in addition to the number of masking steps used for a CMOS process flow.

add G1

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